WHAT IS CLAIMED IS:

1. An integrated circuit chip carrier, comprising:
an electrically insulating substrate having an edge;
at least one internal electrically conductive layer connected to circuit ground, at least a portion of the conductive layer extending to the edge of the substrate; and
a second electrically conductive layer applied to at least a portion of the substrate edge, the internal electrically conductive layer in electrical contact with the second electrically conductive layer.

2. An integrated circuit chip carrier according to claim 1, wherein the substrate is a ceramic material.

3. An integrated circuit chip carrier according to claim 2, wherein the second electrically conductive layer is tungsten.

4. An integrated circuit chip carrier according to claim 2, wherein the second electrically conductive layer is molybdenum.

5. A method for providing electromagnetic interference edge shielding to an integrated circuit chip carrier, the chip carrier including top and bottom surfaces and an edge, and at least one internal electric ground layer, the steps comprising:
exposing at least a portion of the internal ground layer along at least a portion of the substrate edge; and
applying an electrically conductive layer to at least a portion of the substrate edge, the conductive layer being applied over the exposed portion of the ground layer and in electrical contact with said ground layer.

6. A method for providing an integrated circuit chip carrier with electromagnetic interference edge shielding, the steps comprising:

stacking-up a plurality of ceramic green sheets, at least one green sheet having an applied electrically conductive first layer being a circuit ground;

applying heat and pressure to the stack-up to sinter the green sheets into a monolithic structure and to metalize the first conductive layer;

exposing at least a portion of the first conductive layer on the structure edge;

applying a second electrically conductive layer of metalized paste to at least a portion of the structure edge and in electrical contact with the first conductive layer; and

sintering the structure a second time to metalize the paste and to create a consolidated chip carrier.

7. A method for providing an integrated circuit chip carrier with electromagnetic interference edge shielding, according to claim 6, including the step of applying the second conductive layer using a printing process.

8. A method for providing an integrated circuit chip carrier with electromagnetic interference edge shielding, according to claim 6, including the step of applying the second conductive layer using a plating process.

9. A method for providing an integrated circuit chip carrier with electromagnetic interference edge shielding, according to claim 6, including the step of applying the second conductive layer to the entire edge of the substrate.

10. A circuit board comprising:

a substrate having a top surface and a bottom surface, the substrate comprising a thermoplastic polymeric material;
electrical circuitry disposed on the top and bottom surfaces of the substrate;
an electrically grounded planar conductive layer substantially encapsulated by the substrate, the planar conductive layer shielding the electrical circuitry from electromagnetic interference originating on a side of the sheet opposite from the electrical circuitry;
a least a portion of the planar conductive layer extending outward to the edge of the substrate; and

a conductive layer applied on at least a portion of the edge of the substrate, wherein the edge conductive layer is electrically connected to the planar conductive layer, whereby the edge conductive layer and the planar conductive layer are designed to electrically block external EMI emissions.

11. A shielded electric circuit board, comprising:
a planar substrate having a top and bottom surface and an edge;

at least one conductive ground layer internal to the substrate, at least a portion of the ground layer exposed on the substrate edge; and
conductive layer applied to at least a portion of the substrate edge, the conductive layer electrically connected to the ground layer exposed portions.

12. The shielded electric circuit board in accordance with claim 11, wherein the substrate includes at least one internal signal layer, said signal layer being co-planar with the internal ground layer and being electrically insulated from the ground layer and the external surfaces of said substrate.